COMPLEMENTARY METAL-OXIDE SILICON HAVING SILICON AND SILICON GERMANIUM CHANNELS

BACKGROUND

Aspects of the present disclosure relate to FinFET device structures, and more particular aspects relate to making FinFETs having p-channel field-effect transistor (pFET) and n-channel field effect transistor (nFET) regions.

As complementary metal-oxide silicon (CMOS) semiconductor devices and manufacturing processes become smaller, following the trend to reduce the size of channel nodes, channel mobility of electrons becomes more difficult. Different channel materials may be utilized in complementary nFET and pFET devices in order to create controllable, reliable semiconductor devices. Utilizing various techniques, silicon (Si) and silicon germanium (SiGe) content in various regions may be carefully controlled, allowing for reliable and efficient semiconductor device fabrication and structures.

SUMMARY

Embodiments of the present disclosure provide for a method, system, and FET device structure.

One embodiment is directed toward a method. The method includes accessing a silicon germanium on insulator (SGOI) wafer having an nFET region and a pFET region, where the SGOI wafer has a silicon germanium (SiGe) layer of a first germanium (Ge) concentration, the SGOI wafer having a first oxide layer over the nFET and pFET regions. The method also includes removing the first oxide layer over the pFET region in response to accessing the SGOI wafer. The method also includes increasing the first Ge concentration in the SiGe layer of the first Ge concentration in the pFET region to a second Ge concentration in response to removing the first oxide layer over the pFET region. The method also includes removing the first oxide layer over the nFET region in response to increasing the first Ge concentration in the SiGe layer of the first Ge concentration in the pFET region. The method also includes recessing the SiGe layer of the first Ge concentration in the nFET region so that the SiGe layer in the nFET region is in plane with the SiGe layer of the second Ge concentration in the pFET region in response to removing the first oxide layer over the nFET region. The method also includes growing a silicon (Si) layer over the SGOI wafer in the nFET region in response to recessing the SiGe layer of the first Ge concentration in the nFET region. The method also includes growing a SiGe layer of a third concentration in the pFET region in response to growing a Si layer over the nFET region, wherein the SiGe layer of a third concentration is in plane with the grown Si layer in the nFET region.

Another embodiment is directed toward a system. The system includes a fabrication apparatus. The system also includes a fabrication controller. The fabrication controller is communicatively coupled to the fabrication apparatus. The fabrication controller is configured to cause the fabrication apparatus to form a silicon germanium on insulator (SGOI) wafer having nFET and pFET regions by accessing a silicon on insulator (SOI) wafer. The fabrication controller is further configured to cause the fabrication apparatus to form a SGOI wafer having nFET and pFET regions by growing a first silicon germanium (SiGe) layer on the SOI wafer. The fabrication controller is further configured to cause the fabrication apparatus to form a SGOI wafer having nFET and pFET regions by condensing the first SiGe layer on the SOI wafer and stripping resulting oxide layer from SiGe. The fabrication controller is further configured to cause the fabrication apparatus to grow a silicon (Si) layer over the nFET region in response to the fabrication apparatus forming the SGOI wafer having nFET and pFET regions. The fabrication controller is further configured to cause the fabrication apparatus to deposit a second oxide mask over the nFET and pFET regions in response to the fabrication apparatus growing the Si layer over the nFET region. The fabrication controller is further configured to cause the fabrication apparatus to strip the second oxide mask layer over the pFET region in response to the fabrication apparatus depositing a second oxide mask over the nFET and pFET regions. The fabrication controller is further configured to cause the fabrication apparatus to grow a second SiGe layer over the pFET region in response to the fabrication apparatus stripping the second oxide mask layer over the pFET region. The fabrication controller is further configured to cause the fabrication apparatus to strip the second oxide mask over the nFET region in response to the fabrication apparatus growing the second SiGe layer over the pFET region.

Another embodiment is directed toward a FET device. The FET device includes a silicon germanium on insulator (SGOI) wafer having an nFET region and a pFET region, wherein the nFET region includes a Si layer located above a Si_xGe_{1-x} layer; wherein the pFET region includes a Si_zGe_{1-z}, layer located above a Si_yGe_{1-y} layer; and wherein the Si_yGe_{1-y} layer has a germanium (Ge) content equal to or greater than the Si_xGe_{1-x} layer, and the Si_zGe_{1-z} layer has a Ge content greater than the Si_yGe_{1-y} layer.

The above summary is not intended to describe each illustrated embodiment or every implementation of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

The drawings included in the present application are incorporated into, and form part of, the specification. They illustrate embodiments of the present disclosure and, along with the description, serve to explain the principles of the disclosure. The drawings are only illustrative of certain embodiments and do not limit the disclosure.

FIG. **1** depicts a FET fabrication process flowchart, according to various embodiments.

FIG. **2** depicts a FET fabrication process flowchart, according to various embodiments.

FIG. **3** depicts a FET fabrication process flowchart, according to various embodiments.

FIG. **4** depicts a FET fabrication process diagram, according to various embodiments.

FIG. **5**A-**5**P depict steps in a FET fabrication process flow and a final structure, according to various embodiments.

FIG. **6** depicts a block diagram of automated computing machinery, according to various embodiments.

FIG. **7** depicts a block diagram of a FET fabrication system, according to various embodiments.

While the invention is amenable to various modifications and alternative forms, specifics thereof have been shown by way of example in the drawings and will be described in detail. It should be understood, however, that the intention is not to limit the invention to the particular embodiments described. On the contrary, the intention is to cover all